

**IN THE CLAIMS:**

1           1.       (Original) A system integrated circuit that is incorporated into an apparatus  
2 together with a memory device, the memory device storing confidential data, the system  
3 integrated circuit comprising:

4                   a central processing unit;

5                   an access unit for reading and writing to and from the memory device;

6                   an indication unit for performing an indication operation at initialization of the  
7 apparatus, the indication operation indicating to the central processing unit to start up; and

8                   a read control unit for performing a read control operation, the read control  
9 operation controlling the access unit to read the confidential data from the memory device,

10                  wherein the read control operation performed by the read control unit precedes the  
11 indication operation performed by the indication unit.

1           2.       (Original) The system integrated circuit of Claim 1,

2                   wherein the apparatus includes a clock signal generator that starts outputting a  
3 clock signal at the initialization of the apparatus, the clock signal being a time series of clock  
4 pulses,

5                   the system integrated circuit further comprises a counter for counting a number of  
6 clock pulses in the time series outputted by the clock signal generator,

7                   the indication unit performs the indication operation when a count of the counter  
8 reaches a first predetermined value, and

9                   the read control unit performs the read control operation when the count of the  
10 counter reaches a second predetermined value that is smaller than the first predetermined value.

1           3.     (Original) The system integrated circuit of Claim 2,  
2                 wherein the indication operation is to switch an internal reset signal from an  
3     inactive state to an active state.

1           4.     (Original) The system integrated circuit of Claim 3,  
2                 wherein the apparatus includes an external reset signal output unit for switching  
3     an external reset signal from an inactive state to an active state, and  
4                 the counter starts counting the number of the clock pulses when the external reset  
5     signal is switched to the active state.

1           5.     (Original) The system integrated circuit of Claim 1,  
2                 wherein the confidential data is encrypted data obtained by encrypting  
3     identification information relating to the apparatus or a user who operates the apparatus,  
4                 the system integrated circuit further comprises a decryption unit for decrypting  
5     the encrypted data read by the access unit, to obtain the identification information, and  
6                 the central processing unit performs processing using the obtained identification  
7     information, after indicated to start up.

1           6.     (Original) The system integrated circuit of Claim 1,  
2                 wherein the confidential data is a device key that is unique to the memory device,  
3                 the system integrated circuit further comprises an encryption unit for encrypting,  
4     when an instruction to write data is given by the central processing unit, the data using the device  
5     key, and  
6                 the access unit writes the encrypted data to the memory device.

1           7.       (Original) The system integrated circuit of Claim 6,  
2                    wherein the access unit reads the encrypted data from the memory device when an  
3 instruction to read the data is given by the central processing unit, and  
4                    the system integrated circuit further comprises a decryption unit for decrypting  
5 the read encrypted data using the device key.

1           8.       (Original) The system integrated circuit of Claim 7,  
2                    wherein the apparatus includes a reception unit for receiving a broadcast wave,  
3                    the data to be written to the memory device is obtained by the reception unit  
4 receiving the broadcast wave, and has been encrypted according to an encryption method  
5 determined by a broadcaster beforehand, and  
6                    the encryption unit encrypts, using the device key, the obtained data that has been  
7 encrypted, when the instruction to write the data is given by the central processing unit.

1           9.       (Original) The system integrated circuit of Claim 8,  
2                    wherein the decryption unit  
3                    (a)     decrypts the encrypted data that has been read into the system integrated  
4 circuit from the memory device, and  
5                    (b)     further decrypts the resulting data based on the encryption method, to  
6 obtain the data in an original state.

1           10.   (Original) The system integrated circuit of Claim 1,  
2                   wherein the memory device is connected to the system integrated circuit via a bus,  
3   and  
4                   the access unit  
5                   (a)    receives the confidential data via the bus, when the read control operation  
6   is performed by the read control unit, and  
7                   (b)    receives data or an instruction via the bus, when the central processing  
8   unit starts processing.

1           11.   (Original) The system integrated circuit of Claim 1,  
2                   wherein the memory device is connected to the system integrated circuit via a  
3   serial line, and  
4                   the access unit  
5                   (a)    receives the confidential data from the memory device via the serial line,  
6   when the read control operation is performed by the read control unit, and  
7                   (b)    receives data or an instruction from the memory device via the serial line,  
8   when the central processing unit starts processing.

1           12.   (Original) The system integrated circuit of Claim 1,  
2                   wherein the memory device is connected to the system integrated circuit via a bus  
3   and a serial line, and  
4                   the access unit  
5                   (a)    receives the confidential data from the memory device via the serial line,  
6   when the read control operation is performed by the read control unit, and

7                   (b)     receives data or an instruction from the memory device via the bus, when  
8     the central processing unit starts processing.

1           13.     (Original) A system integrated circuit that is connected to a memory device, the  
2     memory device storing confidential data and a program that includes a plurality of instructions,  
3     the system integrated circuit comprising:

4                   a central processing unit for sequentially reading and decoding the instructions  
5     included in the program; and

6                   a storage unit having a plurality of storage regions;

7                   wherein the program includes a first instruction to read the confidential data and a  
8     second instruction to perform processing using the confidential data, the first instruction  
9     preceding the second instruction, and

10                  the system integrated circuit further comprises a read unit for reading the  
11     confidential data from the memory device and writing the read confidential data to a  
12     predetermined one of the storage regions, when the first instruction is decoded by the central  
13     processing unit.